AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph no. 5 on page 1 (bridging pages 1 and 2) with the following amended paragraph:

Along with the progressing micronization of semiconductor devices, there has arisen a problem that a leakage current increases while a transistor is off, ~~because of so called a~~because of a so called short channel effect caused by expansion of a depletion layer around a drain diffusion layer toward a channel. For restraining the short channel effect, up until now an LDD (Lightly Doped Drain) structure has popularly been utilized, whereby an offset gate layer having a lower impurity concentration is formed between a gate and a source or a drain so as to achieve an impurity concentration gradient, and in order to cope with a further micronization of semiconductor devices, a technique of forming a shallow source or drain region (hereinafter briefly referred to as a "source/drain region") in the proximity of a surface of a semiconductor substrate is popularly adopted. Figs. 10A through 10D are cross-sectional process drawings showing a method of manufacturing a conventional semiconductor device.

Please replace the paragraph no. 2 on page 2 (first full paragraph on page 2) with the following amended paragraph:

Initially, a method of manufacturing an ordinary MOS transistor provided with a LDD structure will be described referring to Figs. 10A through 10D. Firstly an element isolation dielectric film 2 is formed on a semiconductor substrate 1 by LOCOS method or trench method

as shown in Fig. 10A, for defining a field region where a MOS transistor is to be formed. Then a gate dielectric film 8 constituted of a silicon oxide layer is formed by thermal oxidation method or the like, after which a polysilicon is deposited by low-pressure (LP) CVD method etc., to thereby form a gate electrode 9 by a known photolithography or a dry etching technique.